SWARNANDHRA
COLLEGE OF ENGINEEERIN G AND TECHNOLGY
(AUTONOMOUS)

SEETHARAMPURAM, NARSAPUR-534280, WG- DT, AP

DEPARTMENT OF MASTER OF COMPUTER APPLICATIONS

TEACHING PLAN

Course Code	Course Title	Year / Sem.	Branch	Contact Hr./ week	Academic Year	Date of Commencement of Semester
20MC1T02	Computer Organization	I/I	MCA	6	2023-24	04.10.2023

COURSE OUTCOMES: Upon the successful completion of this course the student will be able

1. Understand the basic organization of computer and different instruction formats and addressing modes (K2)
2. Analyze the concept of pipelining, segment registers and pin diagram of CPU(K4)
3. Understand and analyze various issues related to memory(K2)
4. Evaluate various modes of data transfer between CPU and I/O Devices(K5)
5. Examine various inter connection structures of multiprocessors(K4)

Unit	OUTOCME Blooms Level	TOPIC/ACTIVITY		Text Book	Contact HOURS	Delivery Method
I	Understand the basic organization of computer and different instruction formats and addressing	**UNIT-I**				Chalk & Board, PPT
		1.1	Computer Types	T1	1	
		1.2	Functional Units	T1	2	
		1.3	Basic Operational Concepts	T1	2	
		1.4	Bus Structures	T1	1	
		1.5	Software	T1	1	

	modes (K2)	1.6	Performance	T1	1	
		1.7	Multiprocessors	T1	1	
		1.8	Multicomputers	T1	1	
		1.9	Historical Perspective	T1	1	
II	Analyze the concept of pipelining, segment registers and pin diagram of CPU (K4)	**UNIT - II**				Chalk & Board PPT, Video
		2.1	Number and Character representation	T1	1	
		2.2	Arithmetic Operations	T1	1	
		2.3	Overflow in Integers, Characters	T1	1	
		2.4	Byte Addressability, Big-endian and Little-endian	T1	1	
		2.5	Word Assignment	T1	1	
		2.6	Memory Operations	T1	1	
		2.7	Register Transfer Notations	T1	1	
		2.8	Instruction Execution	T1	1	
		2.9	Branching and Condition codes	T1	1	
		2.10	Addressing Modes	T1	1	
		2.11	Assembly Languages	T1	1	
		2.12	Basic I/O Operations	T1	1	
		2.13	Stacks and Queues	T1	1	
		2.14	Additional instructions	T1	1	
III	Understand and analyze various issues related to memory (K2)	**UNIT - III**				Chalk & Board PPT Demonstration
		3.1	Accessing I/O Devices	T1	1	
		3.2	Interrupts	T1	1	
		3.3	Controlling Device Requests	T1	1	
		3.4	Use of Interrupts in OS	T1	1	
		3.5	ARM Interrupt Structure	T1	1	
		3.6	Pentium Interrupt Structure	T1	1	
		Mid I Exam				
		3.7	DMA	T1	2	
		3.8	Buses	T1	1	
		3.9	Interface Circuits	T1	2	
		3.10	PCI Bus	T1	1	
		3.11	SCSI Bus	T1	1	
		UNIT - IV				
		4.1	Connection of Memory	T1	1	

IV	Evaluate various modes of data transfer between CPU and I/O Devices (K5)		and Processor			Chalk & Board PPT, Demonstration
		4.2	Semiconductor RAM memories	T1	2	
		4.3	Memory System consideration	T1	1	
		4.4	ROM, PROM	T1	1	
			EPROM, EEPROM, Flash Memories	T1	1	
		4.5	Speed, size and cost	T1	1	
		4.6	Cache memories	T1	2	
		4.7	Performance consideration	T1	2	
		4.8	Virtual memories	T1	1	
		4.9	Memory management requirements	T1	1	
		4.10	Secondary storage	T1	2	
UNIT - V						
V	Examine various inter connection structures of multiprocessors (K4)	5.1	Forms of parallel processing	T1	1	Chalk & Board PPT
		5.2	Array Processing	T1	1	
		5.3	Structure of General purpose Multiprocessors	T1	1	
		5.4	Interconnection Networks: Single Bus,	T1	1	
		5.5	Crossbar Networks	T1	1	
		5.6	Hypercube Networks, Tree Networks	T1	1	
		5.7	Ring Networks	T1	1	
		5.8	Mixed Topology Networks	T1	1	
		5.9	Symmetric Multiprocessors	T1	1	
		5.10	Memory Organization in Multiprocessors	T1	1	
	Course beyond the Syllabus	5.11	Interprocessor Communication	T2	1	
		MID EXAM 2				
		TOTAL CLASSES			65	

Recommended Text Books for Reading:

1. Carl Hamacher, Zvonks Vranesic, Safea Zaky, Computer Organization, 5th Edition, McGraw Hill, 2011.
2. John P. Hayes ,~~3rd. Edition,~~ Computer Architecture and Organization , 3rd Edition McGraw Hill, 2012

Reference Text Books:

1. Alex Holmes, Hadoop in Practice MANNING Publ, 2012
2. Srinath Perera, Thilina Gunarathne Hadoop MapReduce Cookbook, 2013

Faculty **Head of the Department** **Principal**