SWARNANDHRA COLLEGE OF ENGINEEERIN G AND TECHNOLGY (AUTONOMOUS)

SEETHARAMPURAM, NARSAPUR-534280, WG-DT, AP DEPARTMENT OF MASTER OF COMPUTER APPLICATIONS

TEACHING PLAN

Course Code	Course Title	Year / Sem.	Branch	Contact Hr./ week	Academic Year	Date of Commencem ent of Semester
20MC1T02	Computer Organization	1/1	MCA	6	2024-25	26.08.2024

COURSE OUTCOMES: Upon the successful completion of this course the student will be able

- 1. Understand the basic organization of computer and different instruction formats and addressing modes (K2)
- 2. Analyze the concept of pipelining, segment registers and pin diagram of CPU(K4)
- 3. Understand and analyze various issues related to memory(K2)
- 4. Evaluate various modes of data transfer between CPU and I/O Devices(K5)
- 5. Examine various inter connection structures of multiprocessors(K4)

Unit	OUTOCME Blooms Level		TOPIC/ACTIVITY	Text Book	Contact HOURS	Delivery Method	
I	Understand the basic	UNIT-I					
	organization	1.1	Computer Types	T1	1	GL 11	
	of computer	1.2	Functional Units	Tı	2	Chalk	
	and different instruction	1.3	Basic Operational Concepts	Tı	2	& Board,	
	formats and	1.4	Bus Structures	T1	1	PPT	
	addressing	1.5	Software	T1	1		

		4.1	Connection of Memory and Processor	T1	1	
	-	4.1	UNIT - IV			
		J		T1	1	
		3.11	SCSI Bus	T ₁	1	
		3.10	PCI Bus	T1	2	
	-	3.9	Interface Circuits	T ₁	1	ation
	-	3.7 3.8	DMA Buses	T1	2	
	(K2)		Mid I Exam			Demonstr
II	and analyze various issues related to memory		Structure			PPT
		3.6	Pentium Interrupt	T1	1	Board
		3.5	ARM Interrupt Structure	T ₁	1	&
		3.4	Use of Interrupts in OS	T1	1	Chalk
1	Understand	0.0	Requests	11		
		3.3	Controlling Device	T1	1	
		3.2	Interrupts	T1	1	
		3.1	Accessing I/O Devices	T ₁	-	
			UNIT - III	7.7	-	
		2.14	Additional instructions	T1	1	
		2.13	Stacks and Queues	T1	1	
		2.12	Basic I/O Operations	T1	1	
		2.11	Assembly Languages	T1	1	
		2.10	Addressing Modes	T1	1	
			Condition codes		_	PPT, Video
	(K4)	2.9	Branching and	T1	1	
	pin diagram of CPU	2.8	Notations Instruction Execution	T1	1	
11	registers and	2.7	Register Transfer	T1	1	
11	segment	2.6	Memory Operations	T1	1	Board
	pipelining,	2.5	Word Assignment	T1	1	&
	Analyze the concept of	2.4	Byte Addressability, Big- endian and Little-endian	T1	1	Chalk
		2.3	Overflow in Integers, Characters	T1	1	
		2.2	Arithmetic Operations	T1	1	
		2.1	Number and Character representation	T1	1000	
			UNIT - II	rr.	1	
		1.9	Historical Perspective	Tı	1	
		1.8	Multicomputers	T1	1	
	(K2)	1.7	Multiprocessors	T1	10.00	
	modes	1.6	Performance	T1	$\frac{1}{1}$	

	modes	1.6	Performance	Tı	1	-
	(K2)	1.7	Multiprocessors	Tı	1	-
		1.8	Multicomputers	Tı	1	1
		1.9	Historical Perspective	Tı	1	
			UNIT - II			
		2.1	Number and Character representation	Tı	1	
		2.2	Arithmetic Operations	T1	1	
		2.3	Overflow in Integers, Characters	T1	1	
	Analyze the	2.4	Byte Addressability, Big- endian and Little-endian	Т1	1	Chalk
	concept of pipelining,	2.5	Word Assignment	T1	1	&
	segment	2.6	Memory Operations	T ₁	1	Board
11	registers and pin diagram of CPU (K4)	2.7	Register Transfer Notations	Т1	1	PPT, Video
		2.8	Instruction Execution	T1	1	
		2.9	Branching and Condition codes	T1	1	
		2.10	Addressing Modes	T1	1	
		2.11	Assembly Languages	T1	1	
		2.12	Basic I/O Operations	T1	1	
		2.13	Stacks and Queues	T1	1	
		2.14	Additional instructions	T1	1	
		2.14	UNIT - III			1.0
				T1	1	+
	Understand and analyze various issues related to memory (K2)	3.1	Accessing I/O Devices	T1	1	
		3.2	Interrupts Controlling Device	T1	1	-
		3.3	Requests		_	Chalk
		2.4	Use of Interrupts in OS	T1	1	100 PERSONAL PROPERTY.
		3.4 3.5	ARM Interrupt Structure	T1	1	- &
- 1		3.6	Pentium Interrupt	T1	1	Board
		3.0	Structure			PPT
III		Mid I Exam				Demonst
		3.7	DMA	T1	2	ation
		3.8	Buses	T1	1	-
		3.9	Interface Circuits	Tı Tı	1	\dashv
		3.10	PCI Bus	T ₁	1	
		3.11	SCSI Bus	11	1	
+			UNIT - IV			
		4.1	Connection of Memory	T ₁	1	
		,	and Processor			

			TOTAL CLASSES		65	
			MID EXAM 2			
	the Syllabus	5.11	Interprocessor Communication	12		
	Course beyond	5.10	Memory Organization in Multiprocessors	T1	1	
		5.9	Symmetric Multiprocessors	T1	1	
		5.8	Mixed Topology Networks	T1	1	
	(K4)	5.7	Ring Networks	T1	1	
	structures of multiprocessors	5.6	Hypercube Networks, Tree Networks	T1	1	Board PPT
v	various inter	5.5	Crossbar Networks	T1	1	& Record
	Examine	5.4	Interconnection Networks: Single Bus,	T1	1	Chalk
		5.3	Structure of General purpose Multiprocessors	T1	1	
		5.2	Pipeline Processors	T1	1	
		5.1	Basic Concepts	T1	1	
	2/ 1		UNIT - V			11
		4.10	Secondary storage	T1	2	
		4.9	Memory management requirements	T1	1	
		4.8	Virtual memories	T1	1	
	Evaluate various modes of data transfer between CPU and I/O Devices (K5)	4.7	Performance consideration	T1	2	ation
		4.6	Cache memories	T1	2	Demonstr
IV		4.5	Flash Memories Speed, size and cost	T1	1	Board PPT,
			EPROM, EEPROM,	T1	1	&
		4.4	ROM, PROM	T ₁	1	Chalk
		4.3	Memory System consideration	T ₁	1	
		4.2	Semiconductor RAM memories	T1	2	

Recommended Text Books for Reading:

- Carl Hamacher, Zvonks Vranesic, Safea Zaky, Computer Organization, 5th Edition, McGraw Hill, 2011.
- 2. John P. Hayes ,3^{rd.} Edition, Computer Architecture and Organization , McGraw Hill, 2012

Reference Text Books:

- 1. Alex Holmes, Hadoop in Practice MANNING Publ, 2012
- 2. Srinath Perera, Thilina Gunarathne Hadoop MapReduce Cookbook, 2013

Faculty

Head of the Department

Principal