SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)

Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA, Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi, Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ARTIFICIAL INTELLIGENCE AND DATA SCIENCE

TEACHING PLAN

Course Code	Course Title	Semester	Branches	Contact Periods/ Week	Academic Year	Date of Commencement of Semester
23AM4T01	Computer Organization	IV	AI&DS	5	2024-2025	16-12-2024

S.NO	COURSE OUTCOMES
CO1	Identify set of digital components. (K3)
CO2	Demonstrate functional components and micro operations in a basic computer system.(K3)
CO3	Demonstrate various instructions and arithmetic operations.(K3)
CO4	Illustrate knowledge of functional components on central processing unit and various control units.(k2)
CO5	Determine different memory components in a computer for better memory organization.(K3)
CO6	Explain different ways of communication with I/O devices and standard I/O interface.(K2)

Unit	Out Comes / Bloom's Level	Topic No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery Method
UNIT-I: Basic Structure of Computers						
I	CO1: Principles and the Implementation of Computer Arithmetic (K2)	1.1.1	Computer Type	T1	1	Chalk ,talk
		1.1.2	Functional units	T1	1	Chalk ,talk
		1.1.3	Basic operational concepts	T1	1	Chalk ,talk
		1.1.4	Bus structures	T2	1	Web Resources
		1.2.1	Register Transfer Language,	T2	1	Video
		1.2.2	Register Transfer	T1	1	Chalk, talk,
		1.2.3	Bus and Memory Transfers	T1	1	Chalk, talk, PPT
		1.2.4	Arithmetic Micro operations	T1	1	Chalk ,talk
		1.2.5	Logic Micro operations	T1	1	PPT
		1.2.6	Shift Micro operations, Arithmetic Logic Shift Unit.	T1	1	Chalk, talk,PPT
	Content beyond Syllabus	1.2.7	Multiplexers and Decoder connections to be discussed.	T1	1	PPT
				Total	11	
UNIT-II: Basic Computer Organization and Design						
		2.1.1	Instruction Codes, Computer Register	T2	1	Chalk ,talk
		2.1.2	Computer Instructions, Instruction Cycle,	T2	1	Web Resources
		2.1.3	Memory – Reference Instructions	T2	1	Chalk , talk
		2.1.4	Input –Output and Interrupt, Complete	T2	1	Chalk , talk

II	CO2: Operation of CPUs including RTL, ALU, Instruction Cycle, and Busses. (K2)		Computer Description			
		2.2.1	Addition and Subtraction of Signed Numbers	T2	1	Chalk ,talk
		2.2.2	Design of Fast Adders, Multiplication of Positive Numbers,	T2	1	Web Resources
		2.2.3	Signed-operand Multiplication, Fast Multiplication	T3	1	Chalk ,talk
		2.2.4	Integer Division, Floating-Point Numbers and Operations	T3	1	Chalk ,talk, ppt
	Content beyond Syllabus	2.2.5	Half Adder and Full Adder circuit connections with truth table	T1	1	Chalk ,talk
				Total	**9**	
UNIT-III: Central Processing Unit						
III	CO3: Functionality of central processing unit and control units (K4)	3.1.1	General Register Organization	T1	1	Chalk ,talk
		3.1.2	STACK Organization	T1	1	Chalk ,talk
		3.1.3	Instruction Formats	T1	1	PPT
		3.1.4	Addressing Modes, Data Transfer and Manipulation	T1	1	Chalk ,talk
		3.1.5	Execution of a Complete Instruction, Multiple-Bus Organization,	T1	1	PPT
		3.2.1	Control Memory	T3	1	Chalk ,talk
		3.2.2	Address Sequencing	T1	1	Chalk ,talk
		3.2.3	Micro Program example	T1	1	PPT
		3.2.4	Hardwired Control and Micro Programmed Control.	T3	1	NPTEL video
	Content beyond Syllabus	3.2.5	Different memory equipment's on motherboard compared and discussed.	T3	1	Chalk ,talk
				Total	**10**	
UNIT-IV: The Memory Organization						
IV	CO4: Memory System and I/O Organization (K2)	4.1.1	Memory Hierarchy	T1	1	PPT
		4.1.2	Main memory	T1	1	Web Resources
		4.1.3	Auxiliary memory	T1	1	PPT
		4.1.4	Associate Memory	T1	2	Chalk ,talk
		4.1.5	Cache Memory	T1	1	Web Resources
		4.1.6	Virtual memory	T1	2	Web Resources
		4.1.7	Memory Management Requirements	T2	1	Chalk ,talk

		4.1.8	Secondary Storage	T2	1	Web Resources
	Content beyond Syllabus	4.1.9	Explore all secondary storage devices	T1	1	Chalk ,talk, ppt
				Total	**11**	
UNIT-V: Input / Output Organization						
V	CO5: Memory System and I/O Organization (K2)	5.1	Accessing I/O Devices	T1	2	Web Resources
		5.2	Interrupts	T1	1	Web Resources
		5.3	Processor Examples	T1	2	Chalk ,talk, ppt
		5.4	modes of transfers	T1	1	Chalk ,talk, ppt
		5.5	Direct Memory Access	T2	2	Chalk ,talk
		5.6	Buses, Interface Circuits	T2	2	Web Resources
		5.7	Standard I/O Interfaces	T1	2	Web Resources
	Content beyond Syllabus	5.8	Input and output interfaces on computer compared and discussed	T1	1	Web Resources
				Total	**13**	
			CUMULATIVE PROPOSED PERIODS		**54**	

Text Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1	Pynabananda Chskraborty, Computer Organization &Architecture, 1st Edition, Chapman and Hallkrc, 2020.
2	M. M. Mano, Computer System Architecture, 3rd ed., Prentice Hall of India, New Delhi, 2019.
3	Carl Hamacher, ZvonkoVranesic, SafwatZaky, Computer Organization, 5/e, McGraw Hill,2002.
Reference Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1	William Stallings, Computer Organization and Architecture,6th Edition, Pearson,2006.
2	Andrew S. Tanenbaum, Structured Computer Organization, 4th Edition, Pearson,2005.
3	Sivarama P. Dandamudi, Fundamentals of Computer Organization and Design, Springer, 2006.
Web Details	
1	https://nptel.ac.in/courses/106/105/106105163/
2	http://www.cuc.ucc.ie/CS1101/David%20Tarnoff.pdf
3	https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/
4	https://www.javatpoint.com/computer-architecture-vs-computer-organization
5	https://www.tutorialspoint.com/computer-system-organisation
6	https://study.madeeasy.in/subjects/what-is-computer-organization-and-architecture/
7	https://www.nesoacademy.org/cs/09-computer-organization-and-architecture

8	https://sriindu.ac.in/wp-content/uploads/2023/02/R20CSE2102-Computer-Organization-Architecture
9	http://williamstallings.com/ComputerOrganization
10	https://nptel.ac.in/courses/117105078

		Name	Signature with Date
i.	Faculty	Mr. K. satyanarayana	
ii.	Course Coordinator	Dr. G. Sudhakar	
iii.	Module Coordinator	Mr. K.Jai Prakash	
iv.	Programme Coordinator	Dr.B.Rama krishna	

Principal