SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA
Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi,
Permanent Affiliation to JNTUK, Kakinada
SEETHARAMPURAM, W.G.DT., NARSAPUR-534280, (Andhra Pradesh)

DEPARTMENT OFELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branch	Contact Period /Week	Academic Year	Semester Commencement Date
23EC3T03	Switching Theory & Logic Design (R-23)	III	ECE	5	2025-26	09-07-2025

COURSE OUTCOMES

After completion of the course student are able to:

1. Describe the different number systems, generate various binary codes, and implement SOP and POS forms. **(K2)**
2. Illustrate different types of combinational logic circuits.**(K3)**
3. Apply knowledge of flip-flops in designing of Registers and counters.**(K3)**
4. Analyze the methodology for synchronous sequential circuits and realization of state machines.**(K4)**

Unit No	Out Come/Bloom's Level		Topics/Activity	Reference Text book	Contact Periods	Delivery Method
1	CO1: Describe the different number systems, generate various binary codes, and implement SOP & POS forms(K2)		**UNIT I - REVIEW OF NUMBER SYSTEMS & CODES**			Chalk & Talk, PPT & Tutorial.
		1.1	Representation of numbers of different radix	T1,T2,R1	1	
		1.2	Conversation from one radix to another radix	T1,T2,R1	1	
		1.3	r- 1's compliments of signed numbers	T1,T2,R1	1	
		1.4	r's compliments of signed numbers	T1,T2,R1	1	
		1.5	Gray code, 4 bit codes : BCD, Excess-3, 2421, 84-2-1 code etc.	T1,T2,R1	1	
		1.6	Binary to Gray and Gray to Binary code conversion	T1,T2,R1	1	
		1.7	Error detection & correction codes: parity checking, even parity	T1,T2,R1	1	
		1.8	Error detection & correction codes: odd parity, Hamming code	T1,T2,R1	1	
			BOOLEAN THEOREMS AND LOGIC OPERATIONS			
		1.9	Boolean theorems, principle of complementation & duality	T1,R1,R2	1	
		1.10	De-Morgan theorems	T1,R1,R2	1	
		1.11	Logic operations : Design of gates using universal gates	T1,R1,R2	1	

		1.12	Standard SOP and POS Forms,	T1,R1,R2	1	
		1.13	NAND-NAND realizations	T1,R1,R2	1	
		1.14	NOR-NOR realizations	T1,R1,R2	1	
		1.15	Realization of three level logic circuits.	T1,R1,R2	1	
		1.16	Realization of three level logic circuits.	T1,R1,R2	1	
				TOTAL	16	
2	CO2: Illustrate different types of combinational logic circuits.(K3)		**UNIT II -MINIMIZATION TECHNIQUES**			Chalk & Talk, PPT & Tutorial T1,R1,R2
		2.1	Minimization and realization of switching functions using Boolean theorems	T1,R1,R2	1	
		2.2	K-Map (up to 4 variables)	T1,R1,R2	1	
		2.3	K-Map 5 variables	T1,R1,R2	1	
		2.4	K-Map 6 variables	T1,R1,R2	1	
		2.5	Tabular method (Quine mccluskey method) with only four variables and single function.	T1,R1,R2	1	
			COMBINATIONAL LOGIC CIRCUITS DESIGN			
		2.6	Design of Half adder and Full adder	T1,R1,R2	1	
		2.7	Design of Half Subtractor and Full Subtractor	T1,R1,R2	1	
		2.8	Applications of full adders: 4-bit Adder/ Subtractor	T1,R1,R2	1	
		2.9	Applications of full adders: BCD adder	T1,R1,R2	1	
		2.10	Applications of full adders: Excess-3 adder	T1,R1,R2	1	
		2.11	Applications of full adders: Carry look-a-head adder circuit	T1,R1,R2	1	
		2.12	Design of Code converters using K-Map and implement using logic gates	T1,R1,R2	1	
				TOTAL	12	
3	CO2: Illustrate different types of combinational logic circuits.(K3)		**UNIT III - COMBINATIONAL LOGIC CIRCUITS DESIGN USING MSI & LSI**			Chalk & Talk, PPT & Tutorial T1,R1,R2
		3.1	Design of Encoders: Decimal to BCD	T1,R1,R2	1	
		3.2	Design of Decoders: 2-Line to 4-Line	T1,R1,R2	1	
		3.3	Design of Decoders: 3-Line to 8-Line	T1,R1,R2	1	
		3.4	Design of Multiplexer & De-multiplexers	T1,R1,R2	1	
		3.5	Implementation of higher order circuits using lower order circuits	T1,R1,R2	1	
		3.6	Realization of Boolean functions using decoders and multiplexers	T1,R1,R2	1	
		3.7	Design of Priority encoder	T1,R1,R2	1	
		3.8	Design of 4-bit digital comparator and seven segment decoder.	T1,R1,R2	1	
			INTRODUCTION OF PLD's			

		3.9	PLDs: PROM -Basics structure, realization of Boolean functions, Programming table	T1,R1,R2	1	
		3.10	PLDs: PAL -Basics structure, realization of Boolean functions, Programming table	T1,R1,R2	1	
		3.11	PLDs: PLA -Basics structure, realization of Boolean functions, Programming table	T1,R1,R2	1	
		3.12	Comparison of PROM, PAL and PLA	T1,R1,R2	1	
				TOTAL	12	
4	CO3: Apply knowledge of flip-flops in designing of Registers and counters.(K3)	**UNIT IV - SEQUENTIAL CIRCUITS - I**				Chalk & Talk, PPT & Tutorial
		4.1	Classification of sequential circuits (synchronous and asynchronous)	T1,T2,R1	1	
		4.2	Operation of NAND & NOR Latches: SR,D,JK & T	T1,T2,R1	1	
		4.3	Operation of NAND & NOR Flip-Flops: SR&D with truth tables, excitation tables, reset and clear terminals	T1,T2,R1	1	
		4.4	Operation of NAND & NOR Flip-Flops: JK & T with truth tables, excitation tables, reset and clear terminals	T1,T2,R1	1	
		4.5	Master-Slave JK-Flip-Flop	T1,T2,R1	1	
		4.6	Flip-Flop conversions	T1,T2,R1	1	
		4.7	Flip-Flop conversions	T1,T2,R1	1	
		4.8	Design of Ripple counter (Asynchronous counters)	T1,T2,R1	1	
		4.9	Design of Synchronous counters	T1,T2,R1	1	
		4.10	Design of Ring counter and Johnson counter	T1,T2,R1	1	
		4.11	Design of registers: Buffer register, control buffer register,	T1,T2,R1	1	
		4.12	Design of registers: Shift register, bi-directional shift register	T1,T2,R1	1	
		4.13	Design of registers: Universal shift register	T1,T2,R1	1	
				TOTAL	13	
5	CO4: Analyze the methodology for synchronous sequential circuits and realization of state machines.(K4)	**UNIT V - SEQUENTIAL CIRCUITS - II**				
		5.1	Finite state machine: state diagrams, state tables ,reduction of state tables.	T1,T2,R1	1	
		5.2	Analysis of clocked sequential circuits	T1,T2,R1	1	
		5.3	Mealy to Moore conversion	T1,T2,R1	1	
		5.4	Moore to Mealy conversion	T1,T2,R1	1	
		5.5	Realization of sequence generator	T1,T2,R1	1	

	5.6	Design of Clocked Sequential Circuit to detect the given sequence with overlapping	T1,T2,R1	1	
	5.7	Design of Clocked Sequential Circuit to detect the given sequence without overlapping	T1,T2,R1	1	
			TOTAL	7	
Content beyond syllabus		UP DOWN Counter		1	
			TOTAL NO. OF PROPOSED CLASSES	60	

Text Books:

S.No.	AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION
1	Zvi. KOHAVI, Niraj.K.Jha, "Switching and finite automata theory", 3rd Edition, Cambridge University Press,2009
2	Morris Mano, Michael D Ciletti , "Digital Design", 4th edition PHI publication, 2008
3	Hill and Peterson, "Switching theory and logic design", Mc-Graw Hill TMH edition, 2012.

Reference Books:

S.No.	AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION
1	R S Sedha, "Digital electronics", S.Chand & company limited, 2010
2	A. Anand Kumar, "Switching Theory and Logic Design", PHI Learning pvt ltd, 2016.
3	John F.Wakerly, "Digital Design", 4th Ed., Pearson/PHI, 2018.

Web Details

1	www.nptel.ac.in
2	https://www.youtube.com/watch?v=DBTna2ydmC0&list=PLwjK_iyK4LLBC_so3odA64E2MLgIRKafl

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