LESSON PLAN

Course Code	Course Title	Semester	Branch	Periods /Week	Academic Year	Date of Commencement of Semester
23CS3T01	Computer Organization	III	CSE	5	2025-26	14-07-2025

OUTCOMES

CO. No.	COURSE OUTCOMES	Knowledge Level
CO1	Identify set of digital components.	K3
CO2	Demonstrate functional components and micro-operations in a basic computer system.	K3
CO3	Demonstrate various instructions and arithmetic operations.	K3
CO4	Illustrate knowledge of functional components on central processing unit and various control units.	K2
CO5	Determine different memory components in a computer for better memory organization	K3
CO6	Explain different ways of communication with I/O devices and standard I/O interface	K2

Unit	Out Comes / Bloom's Level	Topic No.	Topics/Activity	Textbook/ Reference	Contact Hour	Delivery Method
I	Identify set of digital components [K3] Demonstrate functional components and micro-operations in a basic computer system [K3]		**Basic Structure of Computers**			
		1.1	Computer Types	T2	1	PPT
		1.2	Functional units	T2	1	Chalk, Talk, PPT
		1.3	Basic operational concepts	T2	1	Chalk & Talk
		1.4	Bus structures	T2	1	Chalk, Talk, PPT
			Register Transfer and Micro operations			
		1.5	Register Transfer Language,	T2	1	Chalk & Talk
		1.6	Register Transfer	T1	1	Chalk, Talk & Animation
		1.7	Bus and Memory Transfer	T1	1	Chalk, Talk, PPT
		1.8	Arithmetic Micro operations	T1	1	Chalk & Talk
		1.9	Logic Micro operations	T1	1	PPT
		1.10	Shift Micro operations	T1	1	Chalk & Talk
		1.11	Arithmetic Micro operations	T1	1	Chalk & Talk
		1.12	Arithmetic Logic Shift Unit.	T1	1	PPT
		CBS-1	Multiplexers and Decoder connections to be discussed	W1	1	PPT
					Total	**13**

II	Demonstrate various instructions and arithmetic operations [K3]	**Basic Computer Organization and Design**				
		2.1	Instruction Codes, Computer Register	T1	1	Chalk&Talk
		2.2	Computer Instructions, Instruction Cycle,	T1	1	Chalk&Talk
		2.3	Memory – Reference Instructions	T1	1	Chalk&Talk
		2.4	Input –Output and Interrupt	T1	1	Chalk, Talk & PPT
		2.5	Complete Computer Description	T1	1	PPT
		Computer Arithmetic				
		2.6	Addition and Subtraction of Signed Numbers	T2	1	Chalk&Talk
		2.7	Design of Fast Adders,	T2	1	Chalk&Talk
		2.8	Multiplication of Positive Numbers,	T2	1	Chalk&Talk
		2.9	Signed-operand Multiplication,	T3	1	Chalk&Talk
		2.10	Fast Multiplication	T2	1	Chalk&Talk
		2.11	Integer Division	T3	1	Chalk, Talk & PPT
		2.12	Floating-Point Numbers and Operations	T3	1	Chalk, Talk & PPT
					Total	**12**
III	Illustrate knowledge of functional components on central processing unit and various control units [K2]	**Central Processing Unit**				
		3.1	General Register Organization	T1	1	Chalk&Talk
		3.2	STACK Organization	T1	1	Chalk&Talk
		3.3	Instruction Formats	T1	1	Chalk, Talk & PPT
		3.4	Addressing Modes,	T1	1	Chalk&Talk
		3.5	Data Transfer and Manipulation	T1	1	Chalk&Talk
		3.6	Execution of Complete Instruction	T1	1	Chalk, Talk & PPT
		3.7	Multiple-Bus Organization,	T1	1	Chalk, Talk & PPT
		Micro-Programmed Control				
		3.8	Control Memory	T3	1	Chalk&Talk
		3.9	Address Sequencing	T1	1	Chalk&Talk
		3.10	Micro Program example	T1	1	PPT
		3.11	Hardwired Control and Micro Programmed Control.	T3	1	Flipped Learning
		CBS-2	Different memory equipment's on motherboard compared and discussed	T3	1	PPT
					Total	**12**
IV	Determine different memory components in a computer for better memory organization [K3]	**The Memory Organization**				
		4.1	Memory Hierarchy	T1	1	PPT
		4.2	Main memory	T1	1	Chalk&Talk
		4.3	Auxiliary memory	T1	2	PPT
		4.4	Associate Memory	T1	2	PPT
		4.5	Cache Memory	T1	1	Chalk&Talk
		4.6	Virtual memory	T1	2	Chalk&Talk
		4.7	Memory Management Requirements	T2	1	PPT
		4.8	Secondary Storage	T2	1	PPT
		CBS-3	Explore all secondary storage devices	W1	1	PPT
					Total	**12**

V	Explain different ways of communication with I/O devices and standard I/O interface [K2]	**Input / Output Organization**				
		5.1	Accessing I/O Devices	T1	1	Chalk&Talk
		5.2	Interrupts	T1	2	Chalk&Talk
		5.3	Processor Examples	T1	2	Chalk, Talk & PPT
		5.4	Modes of transfers	T1	1	Chalk, Talk & PPT
		5.5	Direct Memory Access	T2	1	Chalk&Talk
		5.6	Buses, Interface Circuits	T2	1	Chalk, Talk & PPT
		5.7	Standard I/O Interfaces	T1	2	Chalk&Talk
		CBS -4	Input and output interfaces on computer compared and discussed	R1	1	PPT
					Total	**11**
					CUMULATIVE PROPOSED PERIODS	**60**

Where: CBS: Content Beyond Syllabus

Textbooks:	
S.No.	Authors, Book Title, Edition, Publisher, Year of Publication
T1	M. Morris Mano, *Computer System Architecture*, 3rd (Revised) ed., Pearson, 2017
T2	Carl Hamacher; Zvonko Vranesic; Safwat Zaky; Naraig Manjikian, *Computer Organization and Embedded Systems*, 6th ed., McGraw-Hill, 2012
T3	M. Morris Mano; Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog*, 6th ed., Pearson, 2018
Reference Books:	
S.No.	Authors, Book Title, Edition, Publisher, Year of Publication
R1	Computer Organization and Architecture, William Stallings, 6/e, Pearson,2006.
R2	Andrew S. Tanenbaum; Todd Austin, *Structured Computer Organization*, 6th ed., Pearson, 2013
Web Resource Details	
1	https://nptel.ac.in/courses/106/105/106105163/
2	http://www.cuc.ucc.ie/CS1101/David%20Tarnoff.pdf
3	https://www.slideshare.net/slideshow/computer-organization-and-architecture-62126903/62126903?utm

SN	Designation	Name of the Faculty	Signature of the Faculty
1	Faculty I	Dr. S Gopinath	
2	Faculty II	Dr. A M Durga Kumar	
3	Faculty III	Mr. K V Peddi Raju	
4	Faculty IV	Mr. T Prem Kumar	
5	Faculty V	Mr. G Veerendra Kumar	
6	Faculty VI	Mrs. N Suvarna Parvathi Lakshmi	
7	Faculty VI	Mrs. P Anjalee Devi	P. Anjalee devi
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