



# Swarnandhra College of Engineering & Technology

Autonomous and recognized under 2(F) and 12(B) by UGC

Recognized by AICTE, permanently affiliated to JNTUK Kakinada

Accredited by NAAC with 'A' Grade (2<sup>nd</sup> Cycle)

Seetharamapuram, Narsapur – 530280 (Andhra Pradesh)

## DEPARTMENT OF INFORMATION TECHNOLOGY

### TEACHING PLAN

| Course Code | Course Title                          | Semester | Branch | Contact Periods /Week | Academic Year | Date of commencement |
|-------------|---------------------------------------|----------|--------|-----------------------|---------------|----------------------|
| 23IT3T01    | Digital Logic & Computer Organization | III      | IT     | 6                     | 2025-2026     | 14-07-2025           |

#### COURSE OUTCOMES

|   |                                                                                                     |
|---|-----------------------------------------------------------------------------------------------------|
| 1 | Understanding of digital logic principles and computer organization fundamentals (K2)               |
| 2 | Recognize Digital circuits and structure of computers (K1)                                          |
| 3 | Apply the knowledge on computer arithmetic (K3)                                                     |
| 4 | Categorize memory hierarchy concepts (K4)                                                           |
| 5 | Explain input/output systems and their interaction with the CPU ,memory and peripheral devices (K2) |

| UNIT | Out Comes / Bloom's Level | Topics No. | Topics/ Activity                                            | Text Book/ Reference | Contact Hour | Delivery Method           |
|------|---------------------------|------------|-------------------------------------------------------------|----------------------|--------------|---------------------------|
| I    | CO – 1                    | 1.1        | Binary number                                               | T1                   | 1            | Chalk & Board             |
|      |                           | 1.2        | Fixed point representation<br>Floating point representation | T1                   | 1            |                           |
|      |                           | 1.3        | Number base conversions                                     | T1                   | 1            |                           |
|      |                           | 1.4        | Octal and hexadecimal number                                | T1,R1                | 1            | Power point presentations |
|      |                           | 1.5        | Components                                                  | T1                   | 1            | Assignment                |
|      |                           | 1.6        | Signed binary number                                        | T1                   | 1            | Test                      |
|      |                           | 1.7        | Binary codes                                                | T1,R1                | 1            |                           |
|      |                           | 1.8        | Basics logic Functions, logic gates                         | T1,R1                | 1            |                           |
|      |                           | 1.9        | Universal logic gates                                       | T1                   | 1            |                           |



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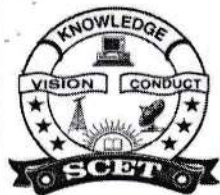
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|       |                         |      |                                               |       |    |                                                                              |
|-------|-------------------------|------|-----------------------------------------------|-------|----|------------------------------------------------------------------------------|
|       |                         | 1.10 | Minimization of logic expressions             | T1    | 1  |                                                                              |
|       |                         | 1.11 | K-MAP simplification                          | T1    | 1  |                                                                              |
|       |                         | 1.12 | Combination circuits                          | T1    | 1  |                                                                              |
|       |                         | 1.13 | Decoder                                       | T1    | 1  |                                                                              |
|       |                         | 1.14 | Multiplexer                                   | T1    | 1  |                                                                              |
|       | Content beyond syllabus | 1.15 | Data representation, digital logic circuits-I | R1    | 1  |                                                                              |
| Total |                         |      |                                               |       | 15 |                                                                              |
| II    | CO – 2                  | 2.1  | Sequential circuits                           | T1,T2 | 1  | Chalk & Board<br><br>Power point presentations<br><br>Assignment<br><br>Test |
|       |                         | 2.2  | Flip- flops                                   | T1,T2 | 1  |                                                                              |
|       |                         | 2.3  | Binary counter                                | T1,T2 | 1  |                                                                              |
|       |                         | 2.4  | Registers                                     | T1,T2 | 1  |                                                                              |
|       |                         | 2.5  | shift registers                               | T1,T2 | 1  |                                                                              |
|       |                         | 2.6  | Computer types                                | T1,T2 | 1  |                                                                              |
|       |                         | 2.7  | Functional units                              | T1,T2 | 1  |                                                                              |
|       |                         | 2.8  | Basics operational concepts                   | T1,T2 | 1  |                                                                              |
|       |                         | 2.9  | Bus structures                                | T1    | 1  |                                                                              |
|       |                         | 2.10 | Software                                      | T1    | 1  |                                                                              |
|       |                         | 2.11 | performance                                   | T1    | 1  |                                                                              |
|       |                         | 2.12 | Multiprocessors and multi computers           | T1,T3 | 1  |                                                                              |
|       |                         | 2.13 | Computer generations                          | T1    | 1  |                                                                              |
|       |                         | 2.14 | Von Neumann architecture                      | T1    | 1  |                                                                              |
|       | Content beyond syllabus | 2.15 | Structure of computers                        | T1    | 1  |                                                                              |
| Total |                         |      |                                               |       | 15 |                                                                              |
| III   | CO – 3                  | 3.1  | Computer arithmetic                           | T1,R1 | 1  | Chalk                                                                        |
|       |                         | 3.2  | Addition and subtraction of signed numbers    | T1,R1 | 1  |                                                                              |
|       |                         | 3.3  | Digital of fast adders                        | T1,R1 | 1  |                                                                              |



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|                         |        |      |                                      |       |    |                                                                              |
|-------------------------|--------|------|--------------------------------------|-------|----|------------------------------------------------------------------------------|
|                         |        |      | number                               |       |    | Board                                                                        |
|                         |        | 3.5  | Signed operand multiplication        | T1,R1 | 1  | Power point presentations                                                    |
|                         |        | 3.6  | Fast multiplication                  | T1,R1 | 1  |                                                                              |
|                         |        | 3.7  | Integer division                     | T1,R1 | 1  | Assignment                                                                   |
|                         |        | 3.8  | Floating point number and operations | T1,R1 | 1  | Test                                                                         |
|                         |        | 3.9  | Fundamental concepts of processor    | T1,R1 | 1  |                                                                              |
|                         |        | 3.10 | Execution of a complete instruction  | T1,R1 | 1  |                                                                              |
|                         |        | 3.11 | Multiple bus organization            | T1,R1 | 1  |                                                                              |
|                         |        | 3.12 | Hard wired control                   | T1,R1 | 1  |                                                                              |
|                         |        | 3.13 | Multi programmed control             | T1,R1 | 1  |                                                                              |
| Content beyond syllabus |        | 3.14 | Computer arithmetic                  | R1    | 1  |                                                                              |
| Total                   |        |      |                                      |       | 14 |                                                                              |
| IV                      | CO – 4 | 4.1  | Introduction Memory organization     | T1,T2 | 1  | Chalk & Board<br><br>Power point presentations<br><br>Assignment<br><br>Test |
|                         |        | 4.2  | Basic concepts of memory             | T1,T2 | 1  |                                                                              |
|                         |        | 4.3  | Semiconductor RAM memories           | T1,T2 | 1  |                                                                              |
|                         |        | 4.4  | Read only memories                   | T1,T2 | 1  |                                                                              |
|                         |        | 4.5  | speed                                | T1,T2 | 1  |                                                                              |
|                         |        | 4.6  | Size and cost                        | T1,T3 | 1  |                                                                              |
|                         |        | 4.7  | Cache memories                       | T1,T3 | 1  |                                                                              |
|                         |        | 4.8  | Performance consideration            | T1    | 1  |                                                                              |
|                         |        | 4.9  | Virtual memories                     | T1    | 1  |                                                                              |
|                         |        | 4.10 | Memory management requirements       | T1    | 1  |                                                                              |
|                         |        | 4.11 | Secondary storage                    | T1    | 1  |                                                                              |
| Content beyond syllabus |        | 4.12 | Memory organization                  | T1    | 1  |                                                                              |
| Total                   |        |      |                                      |       | 12 |                                                                              |
| V                       | CO – 5 | 5.1  | Accessing i/o devices                | T1,R1 | 1  | Chalk & Board<br><br>Power point presentations                               |
|                         |        | 5.2  | Interrupts                           | T1,R1 | 1  |                                                                              |
|                         |        | 5.3  | Processor examples                   | T1,R1 | 1  |                                                                              |
|                         |        | 5.4  | Indirect memory access               | T1,R3 | 1  |                                                                              |



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|                             |     |                           |       |    |                 |
|-----------------------------|-----|---------------------------|-------|----|-----------------|
|                             | 5.5 | Buses                     | T1,R2 | 1  | Assignment Test |
|                             | 5.6 | interface                 | T1,R1 | 1  |                 |
|                             | 5.7 | Standard i/o interfaces   | T1,R1 | 1  |                 |
| Content beyond syllabus     | 5.8 | Input/output organization | R4    | 1  |                 |
| Total                       |     |                           |       | 8  |                 |
| CUMULATIVE PROPOSED PERIODS |     |                           |       | 64 |                 |

## Text Books:

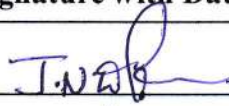
| S.No. | AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION                                                  |
|-------|---------------------------------------------------------------------------------------------------------------|
| 1     | Carl Hamacher, Zvonko Vranesic, Safwat Zaky, <i>Computer Organization</i> , Sixth Edition, McGraw-Hill, 2012. |
| 2     | M. Morris Mano, Michael D. Ciletti, <i>Digital Design</i> , Sixth Edition, Pearson Education, 2017.           |
| 3     | William Stallings, <i>Computer Organization and Architecture</i> , Eleventh Edition, Pearson Education, 2021. |

## Reference Books:

| S.No. | AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION                               |
|-------|--------------------------------------------------------------------------------------------|
| 1     | William stallings, computer organization and architecture, ninth edition, pearson/PH- 2012 |
| 2     | Andrew tanenbaum structured computer organization 6 <sup>TH</sup> edition PHI/pearson-2021 |

## Web Details:

|   |                                                                                                                                                                                                                                                                            |
|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | <a href="https://www.tutorialpoint.com/daa-tutorial">https://www.tutorialpoint.com/daa-tutorial</a>                                                                                                                                                                        |
| 2 | <a href="https://lecturenotes.in/notes/17784-note-for-digital-and-logic-of-computer-organization-daa-by-shekharesh-barik?reading=true">https://lecturenotes.in/notes/17784-note-for-digital-and-logic-of-computer organization - daa-by- shekharesh-barik?reading=true</a> |
| 3 | <a href="https://www.tutorialspoint.com/digital-logic-and-computer-arithmetic/index.htm">https://www.tutorialspoint.com/digital logic and computer arithmetic /index.htm</a>                                                                                               |
| 4 | <a href="https://www.geeksforgeeks.org/#">https://www.geeksforgeeks.org/#</a> computer organization                                                                                                                                                                        |

|                           | Name               | Signature with Date                                                                   |
|---------------------------|--------------------|---------------------------------------------------------------------------------------|
| i Faculty                 | Mrs. J.N.D.Lakshmi |  |
| ii Module Coordinator     | Ms U Jenny Grace   |  |
| iii Programme Coordinator | Dr. RVSV Prasad    |  |

  
Principal