SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA, Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi, Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branches	Contact Periods/ Week	Academic Year	Date of commencement of Semester
23EC6T01	VLSI DESIGN	VI	ECE	5	2025-2026	10-12-2025

COURSE OUTCOMES

After completion of the course students can able to

1	Demonstrate the CMOS fabrication flow and technology scaling (K3)
2	Design basic building blocks in Analog IC design (K4)
3	Construct the various CMOS logic circuits for Combinational and Sequential logic circuits (K3)
4	Analyze the behavior of static and dynamic logic circuits(K4)

UNIT	Out Comes / Bloom's Level	Topics No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery Method
I	CO 1: Demonstrate the CMOS fabrication flow and technology scaling (K3)		**UNIT-1: INTRODUCTION AND BASIC ELECTRICAL PROPERTIES OF MOS CIRCUITS**			
		1.1	Introduction to IC technology & VLSI Design Flow	T1,R1	2	Chalk & Talk, PPT Tutorial, Active Learning & Case Study
		1.2	Fabrication process: nMOS, pMOS and CMOS	T1,R1	5	
		1.3	Ids versus Vds Relationships, Aspects of MOS transistor Threshold Voltage	T1,R1	1	
		1.4	MOS transistor Trans, Output Conductance and Figure of Merit	T1,R1	2	
		1.5	nMOS Inverter, Pull-up to Pull-down Ratio for nMOS inverter driven by another nMOS inverter through one or more pass transistors	T1,R1	2	
		1.6	Alternative forms of pull-up, The CMOS Inverter	T1,R1	1	
		1.7	Latch-up in CMOS circuits,Bi-CMOS Inverter	T1,R1	1	
		1.8	Comparison between CMOS and Bi-	T1,R1	1	

IV	CO3: Construct the various CMOS logic circuits for Combinational and Sequential logic circuits (K3)	**UNIT – 4: CMOS COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUIT DESIGN**				
		Static CMOS Design:				Chalk & Talk, PPT Tutorial
		4.2	Complementary CMOS, Rationed Logic	T1, T3.R1,R2	1	
		4.3	Pass-Transistor Logic, design of Half adder	T1, T3.R1,R2	2	
		4.4	full adder	T1, T3.R1,R2	2	
		4.5	Multiplexer, decoder.	T1, T3.R1,R2	1	
		4.6	Chip level Test Techniques.	T1, T3.R1,R2	1	
		Dynamic CMOS Design:				
			Dynamic Logic-Basic Principles, Speed and Power Dissipation of Dynamic Logic	T3.R1,R2	1	Chalk & Talk, PPT Tutorial
			Issues in Dynamic Design, Cascading Dynamic Gates	T3.R1,R2	1	
			Design examples of sequential circuits: Cross coupled NAND and NOR flip flops	T3.R1,R2	2	
			D flip flop, SR FF	T3.R1,R2	2	
			JK flip flop, SR Master Slave flip flop	T3.R1,R2	2	
				Total	15	
V	CO4: Analyze the behavior of static and dynamic logic circuits(K4)	**UNIT – 5 : FPGA DESIGN**				
		5.1	FPGA design flow	T3.R1,R2	1	Chalk & Talk, PPT Tutorial, Active Learning & Case Study
		5.2	Basic FPG Architecture, FPGA Technologies,	T1,T3,R1	1	
		5.3	Introduction to FPGA Families.	T3,R1,R2	1	
		INTRODUCTION TO ADVANCED TECHNOLOGIES:				
		5.5	Giga-scale dilemma, Short channel effects	T3.R1,R2	1	
		5.6	High–k, Metal Gate Technology	T3.R1,R2	1	
		5.7	Fin FET, TFET	T3,R1,R2	2	
Content beyond the syllabus			CPLD Architecture		1	
				Total	8	
				CUMULATIVE PROPOSED PERIODS	60	

			CMOS technology			
		1.9	MOS Layers, Stick Diagrams	T1,R1,R2	2	
		1.10	Design Rules and Layout	T1,R1,R2	2	
		1.11	Layout Diagrams for MOS circuits	T1,R1,R2	2	
				Total	20	
II	**CO1:** Demonstrate the CMOS fabrication flow and technology scaling (K3)	**UNIT – 2: BASIC CIRCUIT CONCEPTS**				Chalk & Talk, PPT Tutorial, Active Learning & Case Study
		2.1	Sheet Resistance, Sheet Resistance concept applied to MOS transistors and Inverters	T1,R1,R2	2	
		2.2	Area Capacitance of Layers, Standard unit of capacitance, some area Capacitance Calculations,	T1,R1,R2	1	
		2.3	The Delay Unit, Inverter Delays	T1,R1,R2	1	
		2.4	driving large capacitive loads, Propagation Delays,	T1,R1,R2	1	
		2.5	Wiring Capacitances, Choice of layers.	T1,R1,R2	1	
			SCALING OF MOS CIRCUITS			
			Scaling models and scaling factors	T1,R1,R2	1	
			Scaling factors for device parameters	T1,R1,R2	1	
			Limitations of scaling, Limits due to subthreshold currents	T1,R1,R2	1	
			Limits on logic levels and supply voltage due to noise and current density.	T1,R1,R2	1	
				Total	10	
III	**CO2:** Design basic building blocks in Analog IC design (K4)	**UNIT – 3: BASIC BUILDING BLOCKS OFANALOG IC DESIGN**				Chalk & Talk, PPT Tutorial
		3.1	Regions of operation of MOSFET, Modeling of transistor	T2,R2	1	
		3.2	body bias effect, biasing styles	T2,R2	1	
		3.3	single stage amplifier with resistive load	T2,R2	1	
		3.4	single stage amplifier with diode connected load,	T2,R2	1	
		3.5	Common Source amplifier, Common Drain amplifier	T2,R2	2	
		3.6	Common Gate amplifier, current sources and sinks	T2,R2	2	
				Total	8	

Text Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1.	Kamran Eshraghian, Douglas and A. Pucknell And Sholeh Eshraghian "Essentials of VLSI Circuits and Systems"-, Prentice-Hall of India Private Limited, 2005 Edition.
2.	Behzad Razavi, Mc GrawHill "Design of Analog CMOS Integrated Circuits", 2003
3.	Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic "Digital Integrated Circuits", 2nd edition, 2016.
Reference Books:	
S.No.	**AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION**
1.	John P. Uyemura, John Wiley & Sons, "Introduction to VLSI Circuits and Systems", reprint2009
2.	Vinod Kumar Khanna ,"Integrated Nano electronics: Nano scale CMOS, Post-CMOS and Allied Nanotechnologies", Springer India, 1st edition, 2016.
3.	Colinge JP, Editor New York,"Fin FETs and other multi-gate transistors", Springer, 2008.
Web Details	
1.	https://www.vlsisystemdesign.com › basic_courses
2.	https://www.udemy.com › topic › vlsi
3.	https://nptel.ac.in/courses/117101058/

		Name	Signature with Date
i.	Faculty I(for common Course)	Mrs. M.Radha Rani	Radha
ii.	Faculty II	Mr. M.Murali	Murali
iii.	Faculty III	Mrs.V.L.Priyanka	V.L.Priyanka
iv.	Course Coordinator	Mrs. M.Radha Rani	Radha
v.	Module Coordinator	Dr.B.V.Ramana	
vi.	Programme Coordinator	Dr.B.S.Rao	

Swarnandhra College of Engineering & Technology AUTONOMOUS SEETHARAMAPURAM 534 280

Principal
Dr. S.Suresh Kumar

PRINCIPAL
Swarnandhra College of Engineering & Technology
SEETHARAMAPURAM
NARSAPUR - 534 280