SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Accredited by National Board of Accreditation, AICTE, New Delhi,Accredited by NAAC with "A" Grade – 3.32 CGPA,Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi,Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branches	Contact Periods /Week	Academic Year	Date of commenc-ement of Semester
23EC6T02	MICROPROCESSOR AND MICROCONTROLLER ARCHITECTURES	VI	ECE	5	2025-26	10-12-2025

COURSE OUTCOMES: After completion of the course students are able to

CO1	Develop the students to compose the assembly language program for 8086.(K3)
CO2	Applying 8086 processor to interface with necessary peripherals.(K4)
CO3	Analyze the architecture of 8051and interfacing with necessary peripherals.(K4)
CO4	Contrast the introductory concepts of advanced processors, viz. ,ARM processors.(K3)

UNIT	Out Comes / Bloom's Level	Topics No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery Method
I	CO-1: Develop the students to compose the assembly language program for 8086.(K3)	**UNIT-1: INTRODUCTION ,8086 MICROPROCESSORS**				Chalk & Talk, PPT & Tutorial
		1.1	Basic Microprocessor Architecture	T1,R1	**1**	
		1.2	Von-Neumann and Harvard architectures	T1,R1	**1**	
		1.3	Von-Neumann and Harvard architectures examples	T1,R1	**1**	
		1.4	Microprocessor Unit versus Microcontroller Unit	T1,R1	**1**	
		1.5	History and classifications of Microprocessor	T1,R1	**1**	
		1.6	History and classifications of Microcontroller.	T1,R1	**1**	
		1.7	internal architecture of 8086	T1,R1	**1**	
		1.8	register organization	T1,R1	**1**	
		1.9	pin description of 8086	T1,R1	**1**	
		1.10	minimum mode	T1,R1	**1**	

			of 8086 operation and timing diagrams			
		1.11	maximum mode of 8086 operation and timing diagrams	T1,R1	**1**	
		CLASS TEST			**1**	
				Total	**12**	
II	CO-1: Develop the students to compose the assembly language program for 8086.(K3)	**UNIT-2: 8086 PROGRAMMING**				Chalk & Talk, PPT & Tutorial
		2.1	instruction set	T1,R1	**1**	
		2.2	addressing modes	T1,R1	**1**	
		2.3	assembler directives	T1,R1	**1**	
		2.4	programming with an assembler	T1,R1	**1**	
		2.5	Example programs	T1,R1	**1**	
		2.6	stack	T1,R1	**1**	
		2.7	stack structure	T1,R1	**1**	
		2.8	interrupts 8086 system,	T1,R1	**1**	
		2.9	interrupt service routines 8086 system,	T1,R1	**1**	
		CLASS TEST			**1**	
				Total	**11**	
III	CO-2:Applying 8086 processor to interface with necessary peripherals.(K4)	**UNIT-3: 8086 INTERFACING**				Chalk & Talk, PPT & Tutorial
		3.1	Semiconductor memories interfacing RAM	T1,R1	1	
		3.2	Semiconductor memories interfacing ROM	T1,R1	1	
		3.3	Intel 8255 programmable peripheral interface	T1,R1	1	
		3.4	PPI modes of operation	T1,R1	1	
		3.5	Interfacing switches and LEDS, seven segment displays	T1,R1	1	
		3.6	Intel 8251 USART architecture	T1,R1	1	
		3.7	USART interfacing	T1,R1	1	
		3.8	Intel 8237a DMA controller	T1,R1	1	
		3.9	stepper motor	T1,R1	1	Simulation excercises
		3.10	A/D ,D/A converters	T1,R1	1	
		CLAS TEST			1	
				Total	**11**	

IV	CO-3:Analyze the architecture of 8051and interfacing with necessary peripherals.(K4)	**UNIT-4: Intel 8051MICROCONTROLLER and Interfacing**				Chalk & Talk, PPT & Tutorial
		4.1	Architecture	T2,R2	1	
		4.2	Input/output ports and circuits	T2,R2	1	
		4.3	Pin description	T2,R2	1	
		4.4	Internal, external memory	T2,R2	1	
		4.5	counters/timers modes of operation	T2,R2	1	
		4.6	counters/timers modes of operation	T2,R2	1	
		4.7	serial data input/output	T2,R2	1	
		4.8	interrupts	T2,R2	1	
		4.9	instruction set	T2,R2	1	
		4.10	addressing modes	T2,R2	1	
		4.11	Example programs	T2,R2	1	
		4.12	Interfacing to 8051: A/D & D/A Convertors,	T2,R2	1	
		4.12	Stepper motor interface	T2,R2	1	
		4.14	keyboard, LCD Interfacing	T2,R2	1	
		4.16	Traffic light control. Interfacing	T2,R2	1	
		CLASS TEST			1	
				Total	**17**	
V	CO-4: Contrast the introductory concepts of advanced processors, viz. ,ARM processors.(K3)	**UNIT-5: ARM Architectures and Processors**				Chalk & Talk, PPT, Active Learning & Tutorial
		5.1	Introduction to CISC and RISC architectures	T3,R2	1	
		5.2	ARM Architecture	T3,R2	1	
		5.3	ARM Cortex-M Series Family	T3,R2	1	
		5.4	ARM Cortex-M3 Processor Functional Description	T3,R2	1	
		5.5	Instruction set summary	T3,R2	1	
		5.6	System address map	T3,R2	1	
		5.7	write buffer Modes of operation and execution, stack pointer, exceptions and interrupt handling., bit-banding	T3,R2	1	
		5.8	ARM Cortext- programming M3	T3,R2	1	
		5.9	Software delay, Programming techniques	T3,R2	1	
		5.10	Loops, Stack and Stack pointer	T3,R2	1	
		5.11	subroutines and parameter passing, parallel I/O	T3,R2	1	
		5.12	Nested Vectored Interrupt	T3,R2	1	

		5.13	functional description and NVIC programmers' model	T3,R2	1
		CLASS TEST			1
				Total	14
	Content beyond Syllabus		PIC Controller	T2,R1	1
				Total	15
			CUMULATIVE PROPOSED PERIODS		66

Text Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1	A.K.Ray, K.M.Bhurchandi, "Advanced Microprocessors and Peripherals" 3rd edition, Tata McGrawHill, 2017.
2	Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D.McKinlay," The 8051Microcontrollers and Embedded systems Using Assembly and C,; Pearson 2-Edition,2019.
3	JosephYiu.,Newnes-"The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors", Third edition ,Elsevier,2014

Reference Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1	Douglas V Hall, SSSP Rao, Microprocessors and Interfacing – Programming and Hardware, 3rd Edition, Tata McGraw Hill Education Private Limited,2017.
2	Dr.Alexander, G. Dean. "Embedded Systems Fundamentals with Arm Cortex-M based Microcontrollers": A Practical Approach in English, Published by Arm Education Media, 2017

Web Details

1	https://www.tutorialspoint.com/microprocessor/microcontrollers_overview.htm
2	https://circuitdigest.com/article/what-is-the-difference-between-microprocessor-and-microcontroller

		Name	Signature with Date
i.	Faculty I	Mrs. G.B.Christina	
ii.	Faculty II (for common Course)	Mr.I.V.Ravi Kumar	
iii.	Course Coordinator	Mrs. G.B.Christina	
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