

SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY (Autonomous)
 SEETHARAMAPURAM, NARSAPUR-534280 W.G.DT. AP
DEPARTMENT OF BACHELOR OF COMPUTER APPLICATIONS(Honours)

TEACHING PLAN

Course Code	Course Title	Year/Sem	Branch	Contact hr/week	Academic Year
24BC2T04	Computer Organization	I/II	BCA(Honours)	6	2025-2026

Course Objectives:

The purpose of the course is to introduce principles of computer organization and the basic architectural concepts. It provides an in depth understanding of basic organization, design, programming of a simple digital computer, computer arithmetic, instruction set design, micro programmed control unit pipelining and vector processing, memory organization and I/O systems.

Course Outcome(co's) : At the end of the course, student will be able to:

CO No.	Course Outcome	Knowledge Level (K)
CO1	Understand the basic structure of computers, including types, functional units, bus structures, software, performance factors, and data representation methods such as fixed-point and floating-point.	K2
CO2	Apply register transfer language to describe micro-operations including arithmetic, logic, and shift operations, and understand instruction codes, computer registers, and instruction cycles.	K3
CO3	Understand micro programmed control mechanisms and the organization of the central processing unit, including instruction formats, addressing modes, and data manipulation.	K4
CO4	Analyze different types of memory organization, including memory hierarchy, main memory, cache memory, and virtual memory, and understand concepts related to shift registers and RAID.	K4
CO5	Understand the organization of input-output systems, including peripheral devices, interfaces, data transfer modes, priority interrupts, DMA, and serial communication.	K2

Week No	Outcome	Blooms Level	Topic / Activity	Text Books	Contact Hours	Delivery Method	
UNIT-I							
1,2	Understand the basic structure of computers, including types, functional units, bus structures, software, performance factors, and data representation methods such as fixed-point and floating-point.	K2	1.1	Basic Structure Of Computers: Computer Types	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
			1.2	Functional unit	T1	1	
			1.3	Basic Operational concepts	T1	1	
				Bus structures	T1	1	
			1.4	Software	T1	1	
				Performance	T1	1	
			1.5	multiprocessors .	T1	1	
				multi computers.	T1	1	
			1.6	Data Representation.	T1	1	
1.7	Fixed Point Representation.	T1	2				
1.8	Floating – Point Representation.	T1	2				
UNIT-II							
3,4	Apply register transfer languageto describe micro-operations including arithmetic, logic,and shift operations, and understand instruction codes, computer registers,and instruction cycles.	K3	2.1	Register Transfer Language And Micro operations	T1	1	Chalk & Board, PPT , Interactive Whiteboarding
				Register Transfer language.	T1	1	
			2.2	Register Transfer	T1	1	
				Bus transfers	T1	1	
				memory transfers	T1	1	
			2.3	Arithmetic Micro operations	T1	2	
				Logic operations	T1	2	
				shift micro operations	T1	2	
			2.4	Arithmetic logic shift unit.	T1	1	
				Instruction codes	T1	1	
			2.5	Instruction codes, Computer Registers	T1	1	

			2.6	Computer instructions, Instruction cycle.	T1	1	
Mid I Exam							
UNIT-III							
5, 6	Understand micro programmed control mechanisms and the organization of the central processing unit, including instruction formats, addressing modes, and data manipulation.	K4	3.1	Micro Programmed Control: Control memory,	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
			3.2	Addresssequencing	T1	1	
				micro program example	T1	2	
			3.3	design of control unit.	T1	2	
			3.4	Central Processing Unit(Introduction)	T1	1	
				General Register Organization	T1	1	
				Instruction Formats	T1	1	
			3.5	Addressing modes	T1	2	
3.6	Data Transfer and Manipulation	T1	1				
3.7	Program Control.	T1	1				
UNIT-IV							
7,8	Analyze different types of memory organization, including memory hierarchy, main memory, cache memory, and virtual memory, and understand concepts related to shift registers and RAID.	K4	4.1	Memory Organization(Introduction)	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
				Memory Hierarchy	T1	1	
			4.2	Main Memory	T1	2	
			4.3	Auxiliary memory	T1	2	
			4.4	Associate Memory	T1	1	
				Cache Memory	T1	1	
			4.5	Cache memories performance	T1	1	
				performance considerations	T1	1	
			4.6	Virtual memories	T1	1	
			4.7	Introduction to Shift registers	T1	1	
RAID	T1	1					
UNIT-V							
9, 10			5.1	Input-Output Organization(Introduction)	T1	1	
				Peripheral Devices	T1	1	

Understand the organization of input-output systems, including peripheral devices, interfaces, data transfer modes, priority interrupts, DMA, and serial communication	K3	5.2	Input,output,input-output peripherals	T1	1	Chalk & Board, PPT, Interactive Whiteboarding
			Input-Output Interface,	T1	1	
			I/o interface and bus modules	T1	1	
		5.3	Asynchronous data transfer, Modes of Transfer,	T1	1	
			Strobe Control Method	T1	1	
			Handshaking Method	T1	1	
		5.4	Modes of Transfer	T1	1	
			Programmed I/O Interrupt Initiated I/O	T1	1	
			Direct Memory Access	T1	1	
		5.5	Priority Interrupts	T1	1	
			DMA	T1	1	
		5.6	Input-Output Processor	T1	1	
			Serial Communication.	T1	1	
		Mid II Exam				
Total No. of Classes					68	

Recommended Text Books for Reading:

Text Book No	Authors	Title	Edition	Publisher	Year
Text Book 1	Morris Mano	Digital Logic and Computer Design	11th Edition	Pearson Education	1979
Text Book 2	Carl Hamacher, Zvonko Vranesic, Safwat Zaky	Computer Organization	5th Edition	TMH (Tata McGraw-Hill)	2002
Text Book 3	Morris Mano	Computer System Architecture	3rd Edition	Pearson / PHI	1993

Y. Sai Suresh
Faculty

Head of the Department

Principal