SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA, Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi, Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branches	Contact Periods/Week	Academic Year	Date of commencement of Semester
23EC5E01	DIGITAL SYSTEM DESIGN THROUGH HDL	V	ECE-A & B	5	2026-2027	22-06-2026

COURSE OUTCOMES

After completion of the course students can able to

1	Explain the language constructs and programming fundamentals of Verilog HDL (K2)
2	Select appropriate abstraction levels for designing digital circuits (K3)
3	Construct combinational & sequential circuits using different modeling styles in Verilog HDL (K3)
4	Design, simulate and verify the functionality of digital circuits/systems using test benches (K4)

UNIT	Out Comes / Bloom's Level	Topics No.	Topics/Activity	Text Book / Reference	Contact Hour	Delivery Method
I	CO1: Explain the language constructs and programming fundamentals of Verilog HDL (K2)	**UNIT-1: Introduction to Verilog HDL and Gate Level Modelling**				
		1.1	Verilog as HDL, Levels of Design Description	T1,T2	1	Chalk & Talk, PPT & Case Study
		1.2	Basics of Concepts of Verilog,	T1,T2	1	
		1.3	Data Types	T1,T2	1	
		1.4	System Task,	T1,T2	1	
		1.5	Compiler directives,	T1,T2	1	
		1.6	Modules and ports.	T1,T2	1	
		1.7	AND Gate Primitive, Module Structure	T1,R2	1	
		1.8	Other Gate Primitives,	T1,T2	1	
		1.9	Illustrative Examples,	T1,R2	1	
		1.10	Tri-State Gates,	T1,T2	1	
		1.11	Array of Instances of Primitives,	T1,R2	1	
		1.12	Additional Examples,	T1,T2	1	
		1.13	Design of Flipflops with Gate Primitives,	T1,T2	1	
		1.14	Delay	T1,T2	1	
		1.15	Programs examples	T1,R2	1	
				Total	15	
II	CO2: Select appropriate abstraction levels for designing digital circuits (K3)	**UNIT – 2: Behavioral Modelling**				
		2.1	Introduction,	T1,T2	1	Chalk & Talk,
		2.2	Structured procedures	T1,T2	1	
		2.3	procedural assignments,	T1,T2	1	
		2.4	timing controls,	T1,R1	1	
		2.5	conditional statements,	T1,T2	1	

		2.6	multi-way branching,	T1,T2	1	PPT Active Learning & Case Study
		2.7	loops, sequential and parallel blocks	T1,T2	1	
		2.8	generate blocks,	T2,R1	1	
		2.9	Design of Decoders	T1,T2	1	
		2.10	Multiplexers in Behavioral model.	T1,T2	1	
		2.11	Flip-flops in Behavioral model.	T1,T2	1	
		2.12	Registers & Counters in Behavioral model.	T1,T2	1	
			Class Test		1	
				Total	13	
III	**CO2:** Select appropriate abstraction levels for designing digital circuits (K3)	**UNIT – 3: Modelling at Data flow Level**				
		3.1	Introduction,	T1, R1	1	Chalk & Talk, PPT Tutorial
		3.2	Continuous Assignment Structures,	T1, R1	1	
		3.3	Delays and Continuous Assignments,	T1, R1	1	
		3.4	Assignment to Vectors	T1, R1	1	
		3.5	Operators	T1, T2	1	
		3.6	Design of Decoders,	T1, R1	1	
		3.7	Multiplexers	T1, R1	1	
		3.8	Flip-flops in dataflow model	T1, T2	1	
		3.9	Registers & Counters in dataflow model	T1, T2	1	
		3.9	Registers & Counters in dataflow model	T1, T2	1	
			Class Test		1	
				Total	11	
IV	**CO3:** Construct combinational & sequential circuits using different modeling styles in Verilog HDL (K3)	**UNIT – 4: Switch Level Modelling & Synthesis of Logic Gates**				
		4.1	Introduction,	T2, R2	1	Chalk & Talk, PPT Tutorial
		4.2	Basic Transistor Switches,	T1, T2	1	
		4.3	CMOS Switch,	T2, R2	1	
		4.4	Bi-directional Gates,	T2, R2	1	
		4.5	Time Delays with Switch Primitive delays.	T1, T2	1	
		4.6	Introduction to Synthesis.	T1, T2	1	
		4.7	Synthesis of combinational logic,	T2, R2	1	
		4.8	Synthesis of sequential logic with latches and flip-flops	T2, R2	1	
		4.9	Synthesis of sequential logic with latches and flip-flops	T1, T2	1	
			Class Test		1	
				Total	10	
V	**CO4:** Design, simulate and verify the functionality of digital	**UNIT – 5 : Components Test and Verification**				
		5.1	Test Bench – Combinational Circuits Testing,	T2, R2	1	Chalk & Talk, PPT Tutorial
		5.1	Test Bench – Combinational Circuits Testing,	T2, R2	1	

	circuits/systems using test benches (K4)	5.2	Test Bench – Sequential Circuits Testing,	T2, R2	1
		5.2	Test Bench – Sequential Circuits Testing,	T2, R2	1
		5.3	Test Bench Techniques,	T2, R2	1
		5.3	Test Bench Techniques,	T2, R2	1
		5.4	Design Verification,	T2, R2	1
		5.4	Design Verification,	T2, R2	1
		5.5	Assertion Verification	T2, R2	1
			Class Test		1
Content beyond Syllabus (if needed)			User Defined Primitives and FSM Design	T1,T2	1
				Total	11
				CUMULATIVE PROPOSED PERIODS	**60**

Text Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1.	Samir Palnitkar, "Verilog HDL A Guide to Digital and Synthesis" ,2nd Edition, Pearson Education,2006.
2.	Michael, D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson Education India,2005.

Reference Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1.	Padmanabhan, Tripura Sundari -Design through Verilog HDL, Wiley, 2016
2.	S. Brown, Zvonko – Vranesic, Fundamentals of Digital Logic with Verilog Design, TMH, 3rdEdision 2014.
3.	J. Bhasker, A Verilog HDL Primer 2nd edition, BS Publications, 2001.

Web Details

1.	https://www.scribd.com/presentation/70743855/DSD-Using-HDL-co-623-1
2.	https://www.slideshare.net/slideshow/overview-of-digital-design-with-verilog-hdl/248204914

		Name	Signature with Date
i.	Faculty I(for common Course)	Mr.A.R.V.S.Gupta	
ii.	Course Coordinator	Mr.A.R.V.S.Gupta	
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